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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,780	03/23/2004	Susumu Okazaki	1111.70127	2380

7590 06/30/2005

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EXAMINER

A, MINH D

ART UNIT	PAPER NUMBER
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2821

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

10/806,780

**Applicant(s)**

OKAZAKI ET AL.

**Examiner**

Minh D. A

**Art Unit**

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☒ Claim(s) 14 and 15 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 7/15/04.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

**DETAILED ACTION**

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-13 are rejected under 35 U.S.C. 102(b) as being unpatentable by Hirabayashi (US 6,594,064).

Regarding claim 1, Hirabayashi discloses a display device comprising: a first substrate (20) having a plurality of light emitting elements on one surface thereof; and a second substrate (10) having a circuit for controlling the plurality of the light emitting elements, bonded to said one surface of the first substrate (20), and sealing a space where the plurality of the light emitting elements are formed. See figures 1-4, col.6, lines 47-67 to col.13, lines 1-67.

Regarding claim 2, Hirabayashi discloses the circuit including: a plurality of scan bus lines; a plurality of data bus lines intersecting the plurality of the scan bus lines; and a plurality of switching elements arranged respectively at intersections between the plurality of the scan bus lines and the plurality of the data bus lines and electrically connected to the respective plurality of the light emitting elements. See figure 1.

Regarding claim 3, Hirabayashi discloses a plurality of scan bus lines, a plurality of data bus lines intersecting the plurality of the scan bus lines, and a plurality of switching elements arranged respectively at intersections between the plurality of the

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scan bus lines and the plurality of the data bus lines and electrically connected to the respective plurality of the light emitting elements are formed on the first substrate. See figure 1.

Regarding claim 4, Hirabayashi discloses wherein a scan bus line control circuit for controlling signals inputted into the plurality of the scan bus lines, and a data bus line control circuit for controlling signals outputted from the plurality of the data bus lines are formed on the first substrate. See figure 1, col.6, lines 45-67 to col.7, lines 1-60.

Regarding claim 5, Hirabayashi discloses the circuit includes a scan bus line control circuit for controlling signals inputted into the plurality of the scan bus lines, and a data bus line control circuit for controlling signals outputted from the plurality of the data bus lines. See figure 1, col.6, lines 45-67 to col.7, lines 1-60.

Regarding claims 6-8, Hirabayashi discloses the second substrate is a printed circuit board. Col.6, lines 45-67 to col.7, lines 1-60.

Regarding claim 9, Hirabayashi discloses the first substrate and the second substrate are electrically connected to each other by columnar electrodes formed between the first substrate and the second substrate. See figures 1-4.

Regarding claim 10, Hirabayashi discloses the first substrate and the second substrate are electrically connected to each other by a flexible substrate. Col.6, lines 45-67 to col.6, lines 1-65.

Regarding claim 11, Hirabayashi discloses the light emitted by the light emitting elements is taken out toward the other surface of the first substrate. See figures 1-4.

Regarding claim 12, Hirabayashi discloses a plurality of light emitting elements on one surface of a first substrate; forming a plurality of switching elements on one surface of a second substrate; bonding said one surface of the first substrate and said one surface of the second substrate to each other and electrically connecting said respective plurality of the light emitting elements to the respective plurality of the switching elements. See figures 1-4, col.6, lines 47-67 to col.13, lines 1-67.

Regarding claim 13, Hirabayashi discloses one surface of a first substrate a plurality of light emitting elements and a plurality of switching elements electrically connected to said respective plurality of the light emitting elements; forming on one surface of a second substrate a prescribed circuit which is to be electrically connected to said plurality of switching elements; and bonding the first substrate and the second substrate to each other with said one surface of the first substrate and said one surface of the second substrate opposed to each other to electrically connect the circuit to the plurality of the switching elements. See figures 1-4, col.6, lines 47-67 to col.13, lines 1-67.

***Allowable Subject Matter***

3. Claims 14-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art does not teach that, the step of bonding the first substrate and

he second substrate to each other, the first substrate and the second substrate are bonded to each other to seal a space where said plurality of light emitting elements are formed recited in dependent claims 14-15.

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Isami et al (US 6,791,521) and Yamazaki et al . (US 6,563,482) are cited to show a display device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Minh A whose telephone number is (571) 272-1817. The examiner can normally be reached on M-F (5:30 –2:30 PM).

If attempts to reach the examiner by telephone is unsuccessful, the examiner's supervisor, Don Wong, can be reached on (571) 272-1834. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306 for regular communications and (703) 872-9319 for final communications.

Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center receptionist whose telephone number is (571) 272-1553.

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Examiner

Minh A

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6/24/05

  
**TUYET VO**  
**PRIMARY EXAMINER**